

## REMARKS

Reconsideration and further examination are respectfully requested. Claims 1-3 and 5-18 are currently pending.

**Claims 1, 5 & 17:****Rejections under 35 U.S.C. §103**

Claims 1, 5 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Berenbaum et al. (U.S. 7,096,343) in view of Davis et al. (U.S. 5,357,617).

**Berenbaum**

Berenbaum describes, in the abstract:

“...A method and apparatus are disclosed for allocating functional units in a multithreaded very large instruction word (VLIW) processor. The present invention combines the techniques of conventional very long instruction word architectures and conventional multithreaded architectures to reduce execution time within an individual program, as well as across a workload. The present invention utilizes instruction packet splitting to recover some efficiency lost with conventional multithreaded architectures. Instruction packet splitting allows an instruction bundle to be partially issued in one cycle, with the remainder of the bundle issued during a subsequent cycle...”

At column 5, lines 32-34, Berenbaum states ‘a packet containing up to K instructions is fetched each cycle... Thus it is clear that Berenbaum uses the term ‘packet’ to describe a ‘bundle’ of instructions.

In contrast, the claimed invention uses the term ‘packet’ as it is used throughout Application. The term ‘packet’ is a well known term, used in the art to describe a unit of data that is routed between an origin and a destination on the Internet or any other packet-switched network. Applicants have amended the claims to reflect that the term ‘packet’ that is being used is an Internet Protocol packet, *not* a ‘group of instructions’ as described in Berenbaum.

The Examiner states, at page 3 of the office action:

“... Berenbaum discloses method for including instruction packet for each thread of multi-threads system. Berenbaum also discloses method for fetching instruction packets in threads, and sending them to execution pipeline stages: (column 3, lines 1-67; column 4, lines 6-7; column 5, lines 20-67; column 6, lines 5-17; column 7, lines 57-67)...

... Berenbaum discloses method for fetching instruction packets in threads: (column 3, lines 1-67; column 4, lines 6-7; column 5, lines 20-67; column 6, lines 5-17...)”

...Berenbaum does not explicitly disclose processing the first packet in a first stage of a processing pipeline; forwarding the first packet to a next stage of the processing while forwarding the second packet to the first stage of the processing pipeline such that the first packet and second packet can be executed simultaneously in the processing pipeline...”

What Berenbaum in fact describes is fetching ‘a packet containing up to K instructions’ each cycle. (Berenbaum, col. 5, lines 32-34. As described at col. 4, lines 8-20 of Berenbaum:

“..The allocation hardware of the present invention assigns as many instructions from each packet as will fit on the available functional units, rather than allocating all instructions in an instruction packet at one time. Those instructions that cannot be allocated to a functional unit are retained in a ready-to-run register. On subsequent cycles, instruction packets in which all instructions have been issued to functional units are updated from their thread's instruction stream, while instruction packets with instructions that have been held are retained. The functional unit allocation logic can then assign instructions from the newly-loaded instruction packets as well as instructions that were not issued from the retained instruction packets...”

Davis:

Davis describes, in the Abstract:

“... hybrid pipelined processor and associated processing methods ... for separately handling substantially concurrently in a time division manner multiple program instruction threads. The

hybrid architecture includes an instruction fetch unit, an instruction decode unit and an execution unit. The execution unit includes multiple sets of register files each of which contains the working contents for a corresponding one of a plurality n of instruction threads. Timing and control circuitry is coupled to each of the principal processor components for controlling the timing and sequence of operations on instructions from the plurality n of instruction threads such that multiple instruction threads are separately handled substantially concurrently....”

The Examiner states, at pages 3- 4 of the office action:

“... Berenbaum does not explicitly disclose processing the first packet in a first stage of the pipeline; forwarding the first packet to a next stage of the processing while forwarding the second packet to the first stage of the processing pipeline such that the first packet and second packet can be executed simultaneously in the processing pipeline...

In analogous art, Davis discloses a hybrid pipelined processor includes multiple states as fetch stage, decode stage and execution stage. Each of instruction thread moves subsequently from a first stage to the next stage and then keeps going. While one instruction thread moves to the next stage from a first stage, the other instruction thread moves into the first state: (column 2, lines 47-67)...

... it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Davis’ ideas of moving instruction thread subsequently from a first stage to a next stage and then keeps going. While one instruction thread moves to a next stage from a first stage, the other instruction thread moves into the first stage of Berenbaum’s system in order to reduce delay of processing time, see (column 8, lines 10-20).

### **Applicants Argument**

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

No motivation for the Examiner's modification

Although the Examiner states that one would be motivated to modify Berenbaum with the teachings of Davis 'in order to reduce delay of processing time...' Applicants note that it is well known that "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)"

Berenbaum explicitly describes a system wherein an instruction thread is broken into a series of 'packets', with the number of instructions in each packet matching the number of functional units. Allocation logic allocates as many instructions from the packet as will fit on the available functional units in each cycle. "Those instructions that cannot be allocated to a functional unit are retained..."

The Examiner proposes modifying the allocation logic of Berenbaum, which is a critical element of the Berenbaum reference. Applicant respectfully submits that such a modification would change the principle of operation of Berenbaum, and therefore submits that the combination of references fails to satisfy the *prima facie* burden of obviousness.

Combination neither describes nor suggests the claimed invention

As described above, the Berenbaum reference discloses a 'packet' as a 'group of instructions'. Similarly, Davis deals with instruction threads. No mention or suggestion is found in Berenbaum, Davis or the combination thereof of the multi-Internet Protocol (IP) packet

threads of the present invention. In particular, no mention or suggestion is found in Berenbaum, Davis of the combination thereof of the limitations of claim 1, which include:

“...a method for processing a plurality of independent multi-packet threads comprising: retrieving a first Internet Protocol (IP) packet from a first multi-IP packet thread; retrieving a second IP packet from a second multi-IP packet thread; processing the first IP packet in a first stage of a processing pipeline; and forwarding the first IP packet to a next stage of the processing while forwarding the second IP packet to the first stage of the processing pipeline such that the first and the second IP packets can be processed simultaneously in the processing pipeline, and wherein the independence of the multi-IP packet threads eliminates IP packet processing delays...” Independent claims 5 and 17 are also now directed towards a multi-Internet Protocol (IP) packet thread.

Accordingly for the additional reason that the combination of references fails to describe all of the elements of the claims, it is requested that the rejection be withdrawn.

### **Claims 2 & 3:**

Claims 2 & 3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Berenbaum Davis in view of Epps et al. (U.S. 6,813,243).

### **Epps:**

Epps describes, in the Abstract:

“... A pipelined linecard architecture for receiving, modifying, switching, buffering, queuing and dequeuing packets for transmission in a communications network. The linecard has two paths: the receive path, which carries packets into the switch device from the network, and the transmit path, which carries packets from the switch to the network. In the receive path, received packets are processed and switched in an asynchronous, multi-stage pipeline utilizing

programmable data structures for fast table lookup and linked list traversal. The pipelined switch operates on several packets in parallel while determining each packet's routing destination. Once that determination is made, each packet is modified to contain new routing information as well as additional header data to help speed it through the switch. Each packet is then buffered and enqueued for transmission over the switching fabric to the linecard attached to the proper destination port. ..”

Accordingly, for at least the reason that the combination of Berenbaum and Davis do not describe multi-packet threads, the claims are patentably distinct from the references and it is requested that the rejection be withdrawn.

Claims 2&3:

Claims 2&3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Berenbaum/Davis as applied to claims 1 and 5 above, and further in view of Epps et al. (hereinafter Epps) U.S. 6,813,243.

Epps:

Epps describes, in the Abstract: “...A pipelined linecard architecture for receiving, modifying, switching, buffering, queuing and dequeuing packets for transmission in a communications network. The linecard has two paths: the receive path, which carries packets into the switch device from the network, and the transmit path, which carries packets from the switch to the network....”

The Examiner states, at page 5 of the office action ‘it would have been obvious to ... combine Epp’s idea of incorporating processes of transferring data to a packet task manager;

dispatching the data from the packet task manager to an analysis machine; .... with Berenbaum-Davis' system in order to improve the communication rate (Epps, col. 3, lines 39-45).

Applicants first note that col. 3, lines 39-45 of Epps describes a queue congestion control scheme, to be used to provide high throughput; Applicants fail to see how such a teaching of queue congestion control would lead one to modify the architecture of Berenbaum and Davis as suggested by the Examiner.

In addition, Applicants further submit that one would not be motivated to modify Berenbaum Davis in view of the teachings of Epps, because Berenbaum expressly disclose four processing stages as shown in Figure 7B of Fetch, Decode, Allocate and Execute. The modification suggested by the Examiner would fundamentally modify the architectures of Berenbaum and Davis. For at least this reason no motivation can be found for the modification suggested by the Examiner.

Combination neither discloses or suggests the claimed invention

However, even if a motivation could be found, the combination of Berenbaum, Davis and Epps still would neither disclose or suggest the limitations of the claims as described above, because the references, alone and in combination, neither disclose nor suggest 'multi-IP packet threads' as recited in the independent claims.

If an independent claim is nonobvious under **35 U.S.C. 103**, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Although dependent claims 2-4 and 6-18 serve to add further patentable limitations to their parent independent claims, they are patentable for at least the same reasons as their parent claims, and it is respectfully requested therefore that this rejection be withdrawn.

Claims 6-16 and 18:

Claims 6-16 & 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Berenbaum-Davis in view of Epps and further in view of Eickemeyer.

Eickemeyer:

Eickemeyer describes, in the abstract:

“In a simultaneous multithread processor, a flush mechanism of a shared pipeline stage is disclosed. In the preferred embodiment, the shared pipeline stage happens to be one or all of the fetch stage, the decode stage, and/or the dispatch stage and the flush mechanism flushes instructions at the dispatch stage and earlier stages. The dispatch flush mechanism detects when an instruction of a particular thread is stalled at the dispatch stage of the pipelined processor. Subsequent instructions of that thread are flushed from all pipeline stages of the processor up to and including the dispatch stage...”

Thus, like Berenbaum and Davis, Eickemeyer describes a particular architecture of a multi-thread processor. Although the Examiner states ‘it would have been obvious to a person of ordinary skill in the art .... to combine Eickemeyer’s ideas including multiple pipelines in a system with Berenbaum-Davis-Epp’s system in order to provide a flexible multithreads communication system (see Eickemeyer: col. 9, lines 18-41), Applicants would submit that the modifications suggested by the Examiner are not straightforward; rather the Examiner is suggesting changing the fundamental teachings of each of the previous architectures, and that no motivation for such a modification can be found in the references.

In addition, even if a motivation could be found, the modification still would not teach or suggest all of the limitations of the claims. For at least this reason it is requested that the rejection of the claims be withdrawn and the case be allowed to issue...



Conclusions:

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at the number listed below so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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